REMARKS/ARGUMENTS

In the Office Action mailed July 3, 2008, claims 1-5 were rejected. In response, claims 1 and 4 have been amended. Additionally, claims 6-13 have been added. Applicant hereby requests reconsideration of the application in view of amended claims, the new claims, and the below-provided remarks.

Claim Rejections under 35 U.S.C. 102

Claims 1-5 were rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Birns et al. (EP 1,087,298 (A1), hereafter "Birns"). Applicant respectfully submits that the pending claims are not anticipated by Birns for the reasons provided below.

Independent Claim 1

Claim 1 has been amended to include the limitation "*wherein a physical access address of the physical memory comprises least significant bits from a logical address of a message-object memory and least significant bits from a logical byte address within the message-object memory*." Support for the amendment is found in Applicant's specification at, for example, page 7, lines 11-19. Applicant respectfully asserts that Birns does not disclose the above-identified limitation.

Birns discloses that each message object is assigned a message buffer, where the location and the size of the message buffer is programmable, see paragraph [0008]. Birns further discloses that the most significant address bits, such as the upper 8 bits of a 24-bit address of each message buffer, define a location of a memory page in which all message buffers are contained, see paragraphs [0030] and [0045]. Birns also discloses that the least significant address bits, such as the lower 16 bits of the 24-bit address of each message buffer, define the location of the selected message buffer within the memory page, see paragraph [0030] and [0045]. That is, Birns discloses that an address of a message buffer includes a location of a memory page in which all message buffers are contained and a location of the message buffer within the memory page. However, Birns does not disclose that a physical access address of a physical memory location includes least significant bits from a byte address within a message buffer. Because Birns does

not disclose that a physical access address of a physical memory location includes least significant bits from a byte address within a message buffer, Birns does not disclose that "*a physical access address of the physical memory comprises least significant bits from a logical address of a message-object memory and least significant bits from a logical byte address within the message-object memory*," as recited in amended claim 1.

Because Birns does not disclose all of the limitations of amended claim 1, Applicant respectfully asserts that claim 1 is not anticipated by Birns.

Dependent Claims 2, 3, and 5

Claims 2, 3, and 5 depend from and incorporate all of the limitations of amended independent claim 1. Thus, Applicant respectfully asserts that claims 2, 3, and 5 are allowable at least based on an allowable amended claim 1.

Independent Claim 4

Claim 4 has been amended to include the limitation "*wherein a physical access address of the physical memory comprises least significant bits from a logical address of a message-object memory and least significant bits from a logical byte address within the message-object memory*." Support for the amendment is found in Applicant's specification at, for example, page 7, lines 11-19. Amended claim 4 includes similar limitations to amended claim 1. Because of the similarities between amended claim 4 and amended claim 1, Applicant respectfully asserts that the remarks provided above with regard to amended claim 1 apply also to amended claim 4. Accordingly, Applicant respectfully asserts that amended claim 4 is not anticipated by Birns.

New Claims 6-13

Claims 6-13 have been added. Support for claims 6-11 is found in Applicant's specification at, for example, page 7, lines 20-34. Support for claim 12 is found in Applicant's specification at, for example, page 7, lines 16-19. Support for claim 13 is found in Applicant's specification at, for example, page 8, lines 1-4.

Claims 6-8 depend from and incorporate all of the limitations of the independent claim 1. Thus, Applicant respectfully asserts that claims 6-8 are allowable at least based

on an allowable claim 1. Claims 9-11 depend from and incorporate all of the limitations of the independent claim 4. Thus, Applicant respectfully asserts that claims 9-11 are allowable at least based on an allowable claim 4. Additionally, claims 6-11 may be allowable for further reasons respectively, as described below.

Claims 6 and 9 include the limitation that "*the physical access address of the physical memory comprises the five least significant bits from the logical address of the message-object memory and the three least significant bits from the logical byte address within the message-object memory*" (emphasis added). Claims 7 and 10 include the limitation that "*the physical access address of the physical memory comprises the three least significant bits from the logical address of the message-object memory and the five least significant bits from the logical byte address within the message-object memory*" (emphasis added). Claims 8 and 11 include the limitation that "*the physical access address of the physical memory comprises the two least significant bits from the logical address of the message-object memory and the six least significant bits from the logical byte address within the message-object memory*" (emphasis added). Applicant respectfully asserts that Birns does not disclose any of these limitations.

Independent claim 12 includes the limitation that "*the number of address bits of a logical address of a message-object memory and the number of address bits of a logical byte address within the message-object memory are determined by the maximum upper limit of an address space of the message memory.*" Applicant respectfully asserts that Birns does not disclose the above-identified limitation.

Claim 13 depends from and incorporates all of the limitations of the independent claim 12. Thus, Applicant respectfully asserts that claim 13 is allowable at least based on an allowable claim 12. Additionally, claim 13 includes the limitation that "*an access of a protocol controller or of a central processing unit interface to the message memory takes place via the logical, virtual memory representation independently of the configuration of a) logical addresses of the configurable number of message-object memories and b) logical byte addresses within the configurable number of message-object memories.*" Applicant respectfully asserts that Birns does not disclose the above-identified limitation.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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